Performance comparison of CMOS and FINFET based SRAM for 22nm Technology

Lourts Deepak A and Likhitha Dhulipalla
Department of ECE,
M S Ramaiah School of Advanced Studies,
Bangalore, Inida.
{lourdu.lourdu, likhitha.ec}@gmail.com

Dr. Cyril Prasanna Raj P
Professor & Head, Department of EEE,
M S Ramaiah School of Advanced Studies,
Bangalore, India.
cyrilyahoo@gmail.com

Abstract— **As CMOS devices are shrinking to nanometer regime, increasing the consequences in short channel effects and variations in the process parameters which lead to cause the reliability of the circuit as well as performance. To solve these issues of CMOS, FINFET is one of the promising and better technologies without sacrificing reliability and performance for its applications and the circuit design. In this paper we aimed to evaluate and compare the performance of CMOS and FINFET based 6T SRAM cell in 22nm technology. The Predictive Technology Model (PTM) is used to simulate these CMOS and FINFET based SRAM which is a tentative model from Arizona State University. Since the dimensions of the MOSFETs are deduced considerably, it is necessary to know the potential of both technologies, with its available least dimensions. The 6T SRAM design is vulnerable to reliability issues and process variations, making it an ideal design to compare these two technologies. Our simulation result shows that FINFET based SRAM design is a feasible design in contrast with CMOS based SRAM design. The result shows that the signal noise margin (SNM) is increased 25.3% in memory cell and it becomes 5% faster than CMOS based SRAM. This comparison study will help us to select the better and alternative technology to design the circuits in future.**

Keywords- FINFET's, CMOS Vs FINFET, 6T SRAM design

I. INTRODUCTION

The past 3 decades CMOS IC technologies have been scaled down continuously and entered into the nanometer region. In many designs the need of memory has increased vastly from consumer goods to industrial applications. It increases the necessity of improving memories in a single chip with the help of nanometer technologies. There are lots of applications and integrated memories are improved using nanotechnology especially SRAM cell.

The shrinking of the CMOS technology has been increased very aggressively with ultra-thin sizes. This shrinking of the design creates many significant challenges and reliability issues in design which causes augmented process variations, short channel effects, power densities and leakage currents etc. Ultra thin sized CMOS technologies have been designed to use in many applications. Continuous shrinking of channel length is increases the high speed devices in very large scale circuits. This steady miniaturization of transistor with each new generation of bulk CMOS technology has yielded continual improvement in the performance of digital circuits. The scaling of bulk CMOS, however, faces significant challenges in the future due to the fundamental material and the process technology limits. The 22 nm FINFET based transistors are used as choice and solution for CMOS based technology with scaled device geometry. In these device structures, the effect of short-channel length can be controlled by limiting the off-state leakage. Moreover, FINFETs has advantages of suppressing short channel effects, gate-dielectric leakage currents etc.

Here, the Static Random Access Memory (SRAM) is used as an ideal design to compare these two technologies. We used conventional 6T SRAM cell design to compare the highlighted technologies such as based on CMOS and FINFET's. Another reason to chosen the SRAM design is sensitive to transistor density with the help of less number of transistors as possible and reliability problems. We have used spice coding to develop the SRAM and simulated using HSPICE tool.

The paper is organized as follows. Section II gives a short description about the FINFET based model with its different modes. Section III describes about characteristics of FINFET current and voltage under different PVT conditions and compared with CMOS based design. Section IV describes the conventional CMOS 6T SRAM structure as well as FINFET based 6T SRAM structure which illustrate some important design constraints and parameters. Section V and VI explains about simulation result and conclusion of the paper respectively.

II. FIN BASED FIELD EFFECT TRANSISTOR MODES AND DEVICE MODEL PARAMETERS

The continuous down in scaling of bulk CMOS creates major issues due to its base material and process technology limitations. The main drawback of CMOS based design is the leakage in small channel size; due to this the leakage stems increased from the lower oxide thickness, more substrate dopings. The optimal performance of the device can be achieved by lowering the threshold voltage with low supply voltage worsen the leakage. The primary obstacles to the scaling of CMOS gate lengths to 22nm and beyond includes short channel effects, sub-threshold leakage, gate-dielectric leakage and device to device variation reduction which leads

low yield. The International Technology Roadmap for Semiconductors (ITRS) predicts that double gate or multi-gate devices will be the perfect solution to obtain the device with reduced leakage problems and less channel length of the transistor. The FINFET based designs are known as double gate device which offers the better control over short channel effects, low leakage current and better yield in 22nm and beyond which helps to overcome the obstacles in scaling [1][2].

When threshold voltage *Vt* is less than a potential voltage, gates of the double gate or FINFET device activates the currently flow between drain to source with modulating the channel from both the sides instead of one side. The potential which is applied to two gates together influence potential of the channel which fighting against the drain impact and leads to solve and give the better shut off to the channel current and reduces Drain Induced Barrier Lowering (DIBL) with improved swing of the design.

This FINFET based transistors offers good trade off for power as well offering interesting delay. The Figure 1 shows the 3D structure of multi-FIN based field effect transistors. The FINFET model structure consists of following regions.

- ✓ Low doping silicon fin
- ✓ Highly doped poly-silicon region,
- ✓ Highly doped contact region between source and drain
- ✓ Gate region- oxide (SiO_2)

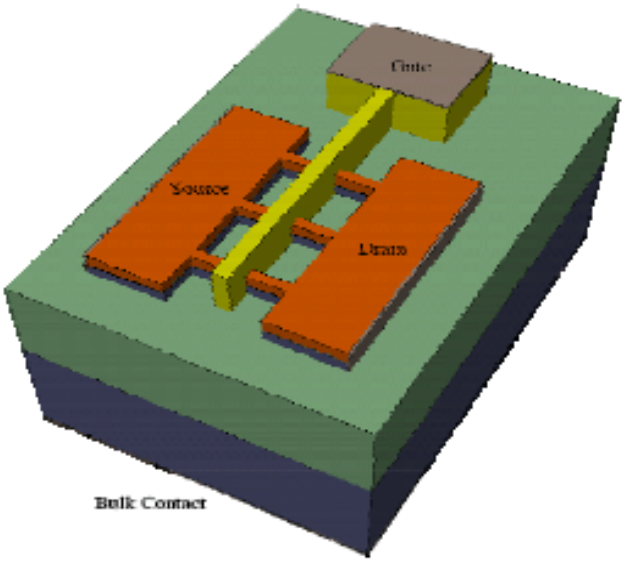

Figure 1. 3D Multi-FIN Based Field Effect Transistor Structure

A. Modes of FINFETs

Double Gate (DG) devices have been used in a variety of innovative ways in digital and analog circuit designs. A parallel transistor pair consists of two transistors with their source and drain terminals tied together. In Double-Gate (DG) FINFETS, the second gate is added opposite to the traditional gate, which has been recognized for their potential to better control short-channel effects, as well as to control leakage current.

The modes of FINFETs are identified as short gate (SG) mode with transistor gates tied together, the independent gate (IG) mode where independent digital signals are used to drive the two device gates, the low-power (LP) mode where the back-gate is tied to a reverse-bias voltage to reduce leakage power and the hybrid (IG/LP) mode, which employs a combination of low power and independent gate modes. Here independent control of front and back gate in DG FINFET can be effectively used to improve performance and reduce power consumption. Independent gate control is used to combine parallel transistors in non-critical paths.

B. FINFET Device Modelling Parameters

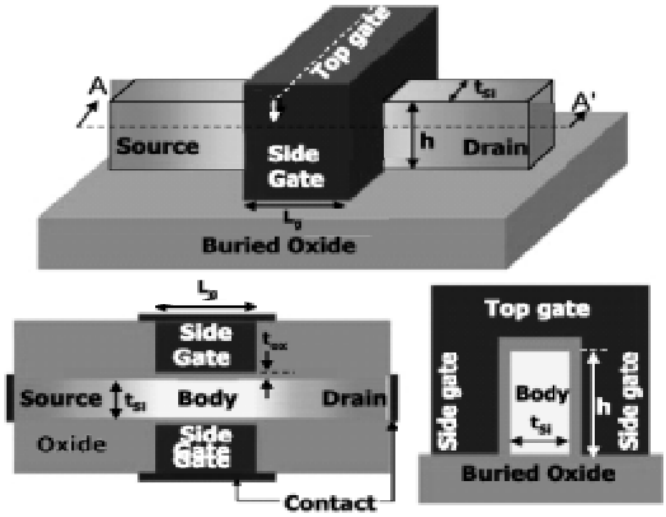

Figure 2. Modeling parameters of FINFET

The FINFET is originally known as the folded channel MOSFET [3] which has narrow vertical fins from wafer. Usually width of the gate will be double of the fin height in FINFETs. FINFETs are nominated instead of CMOS in less than 22nm technology due to its cost effective manufacturing. The geometric key parameters of FINFETs are

i) L_g – Length of the gate,

ii) h – Height of the FIN,

iii) t_{ox} – Thickness of gate oxide,

iv) $t_{ox\text{-}top}$ - Oxide thickness of top gate and fin,

v) T_{si}- Thickness of the fin

vi) Channel Doping.

These parameters are playing an important role in minimizing the I_{off} leakage current and maximize the I_{on} current. Height of the fin should be same all over the chip to avoid the process complications and reduce the defects. Height balancing, thickness of fin, thickness of oxide and channel length should be balanced based on the FIN engineering. The Figure 2 shows the modeling parameters of FINFETs. The

table 1 shows the comparison of device parameters for nominal 22nm FINFET and CMOS NMOS and PMOS devices. To study about the FINFET circuit behavior, we have used HSPICE simulation tool from Synopsys to analyze the FINFET based NMOS transistor. Other than these parameters, some other parameters also an important which is mentioned below with its calculation:

Effective Channel Length (L_{effg}):- Most of the scaling behavior of FINFET is not equal to poly length L_g which is very significant, but the effective channel length $L_{effg} = L_g - \Delta L$. Generally effective length of the transistor can be extracted from measurement or simulation result. But it isn't a reliable technique. The reliable technique is, by looking the total oxide capacitance C_{ox} as a function of L_g. Since the FINFETs are floating body device, it is difficult to find the effective channel length from the simulation/measurement. The following formulae is used to find the C_{ox}

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} W_{eff} (L_g - \Delta L)$$

Gate Capacitance (C_g):- It can be calculated using the following formulae:

$$C_g = C_0 W L$$

Where C_0 is the gate capacitance per unit are which is mentioned below:

$$C_0 = \epsilon_r \epsilon_o / D$$

Here, D – Thickness of gate oxide,
W – Width of the Channel
L – Length of the Channel
$\epsilon_r \epsilon_o$ – Relative permittivity

Channel Resistance (R_C): - It can be calculated as follows:

$$R_C = L / W Q_{on} x \mu$$

Where, $Q_{on} = C_0 x V_{gs}$

μ - is Constant carrier mobility

TABLE I. COMPARISON OF DEVICE PARAMETERS FOR NMOS AND PMOS BASED FINFET DEVICE

Device Parameters	FINFET		Bulk CMOS	
	N MOS	P MOS	N MOS	P MOS
Gate Length (L_g)	22 nm	22 nm	22 nm	22 nm
Thickness of Fin & Channel (t_{si})	8nm	8nm	8.6 nm	8.6 nm
Thickness of Oxide (t_{ox})	1.05nm	1.1 nm	1.4 nm	1.4 nm
Height of the FIN	16 nm	16 nm	-	-
Channel doping (cm^{-3})	10^{16}		$4x10^{18}$	
Supply voltage	0.8 V		0.9 V	

Gate Delay (T_d): - delay of the gate can be calculated as

$$T_d = R_{on} x C_g$$

Where, C_g - Gate capacitance

These values like Gate capacitance, Charge per unit area, Gate capacitance per unit area, Gate delay and Channel resistance can be obtained by adjusting the Oxide thickness [4].

III. CHARACTERISTICS OF FINFET

Based on the model parameters explained in section II, it is necessary to be familiar with the characteristics of FINFET based transistors. The basic characteristics of FINFET are identified in terms of current and voltage across a transistor. The Figure 3 shows the *Vt* roll on comparison between FINFET and Planer based FET. Another advantage of FINFET is the controlling of threshold voltage in high-k/Metal gate stack. To obtain the comparable *Vt* at long gate length with planar FETs that use dual capping layer and high channel dopant concentration is not necessary for FINFET to suppress the SCE [5]. This leads the simpler process integration of the FINFETs. The drain to source current is basically depends on the process, temperature and voltage. Mobility carrier and threshold voltage decreases as voltage or temperature increase which causes the reduction in drain current.

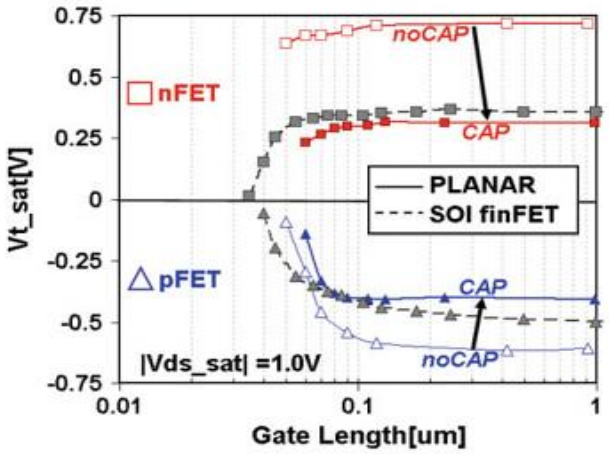

Figure 3. Comparison between FINFET and CMOS [5]

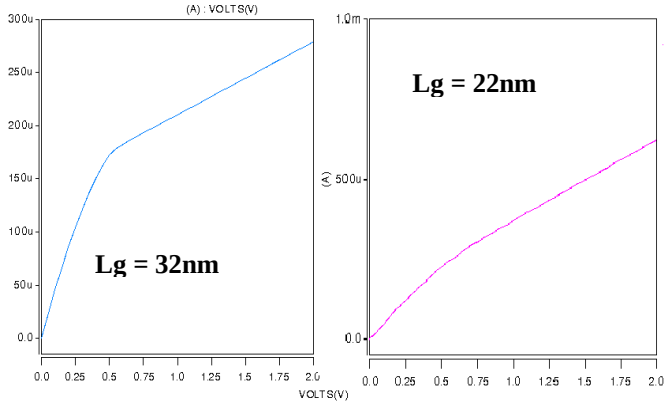

Figure 4. I-V Characteristics Curve for 32 and 22nm NMOS FINFET

The Figure 4 shows the I-V characteristic curve of NMOS transistor in 22 nm technology for Vg =1 and 0.5V. From this characteristic curve, we can say that the current increases linearly with increase in voltage. The point where the current remains almost constant is the point where the FINFET reaches the saturation. This point is called as threshold voltage of NMOS based FINFET.

The above Figure has developed to analyze the I-V characteristic curve for 32 nm technology and 22nm technology with 16nm fin thickness which resulting the faster switching of 22nm compared with 32nm. The table 2 shows the drain current of Short Gated (SG) mode (highlighted in blue) and Independent Gate (IG) mode (highlighted in green) with different front gate bias (V_{FG}) back gate bias (V_{BG}).

TABLE II. IDS COMPARISON OF FINFET SG/IG MODES

SG(V_{BG} = V_{FG}) / IG (V_{BG} = 0.0)	**V_{DS} (V)**	**V_{FG}(V)**	**V_{BG}(V)**	**I_{DS}(A)**
Saturation current	1.0	1.0	1.0	30 µ
Linear current	0.1	1.0	1.0	19 µ
Off current	1.0	0.0	0.0	0.04n
High V_{DS}	1.0	1.0	0.0	14 µ
Low V_{DS}	0.1	1.0	0.0	7 µ

IV. 6-TRANSISTOR SRAM DESIGN [6]

The SRAM cell is one of the promising application of FINFET based design, the Figure 5 is shows the 6 transistor model based on FINFET where the each gate of FINFET controlled independently. The SRAM cell consists of two CMOS inverters (M1, M2 and M3, M4) where the output of each is fed as input to each other; this loop is used to stabilize the inverters to their respective state.

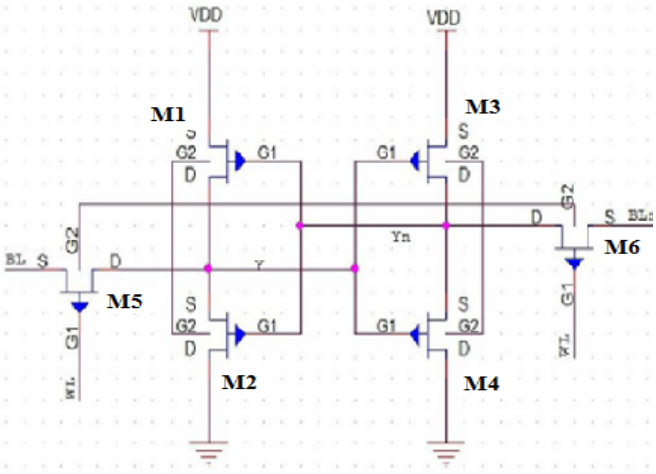

Figure 5. 6T SRAM cell using FINFET

The access transistors (M5 and M6) and the word and bit lines WL and BL are used to write and read, to and from the cell. In the standby mode the access transistors turn OFF by making the word line low. The inverter output will be complementary in this state. The PMOS of the left inverter is turned ON, the output potential is high and the PMOS of the second inverter is switched to OFF. The gates of the transistor that connect the bit line and the lines of the inverter are driven by the word line. Keeping the word line low is used to disconnect the SRAM cell from the bit lines. For better operation of cell it is necessary to do the proper transistor sizing of the cell with respect to the requirements. For multi-fin devices, the electrical width of a FINFET with *N* number of fins can be calculated using the following formulae $W = 2 * N * h$. Width quantization of fin in FINFET based design is used to ensure the stability of the memory circuit with fine control of transistor drive strength.

A. Read and Write operation of SRAM Cell

The word line high makes the NMOS conduct and connect the inverter inputs and outputs to two vertical bit lines. These inverters drive the current value stored inside the memory cell onto the bit line and inverted the value on the inverted bit line, this data generates the output value of the SRAM cell during a read operation.

In writing operation, the strong bit lines are activated by input drivers to write the data into the memory. Depending on the current value there might be a short circuit condition and the value in SRAM is overwritten. The above mentioned Figure 2 shows the simulation output of read and write operation for 1-bit 6T SRAM cell.

V. SIMULATION RESULTS

The 22nm FINFET based SRAM cell has been developed using the spice code and it is analyzed through the Synopsys spice software tool HSPICE with the help of 22nm Predictive Technology Models which is obtained from ptm.asu.edu. It consists of parameters value for 22nm technology related, the length of gate taken as 22nm to synthesize the result for 6T SRAM cell. The transistor size for the SRAM cell has been calculated and described in the table 3.

TABLE 3. TRANSISTOR SIZING OF 6T SRAM CELL

Transistors	**M1 & M3**	**M2 & M4**	**M5 & M6**
Size	90 nm	120 nm	180 nm

The spice code for 1-bit 6T SRAM has developed using short gated mode since it can able to give better performance under all the load conditions with high speed, whereas the independent gate mode method gives slow performance with low leakage and low switched capacitance. The table 4 shows the summarized simulation result of SG mode and IG mode SRAM.

From the above simulation summary, the short gated mode FINFET has good advantage over IG mode and CMOS based 6T SRAM cell. The delays of IG mode read and write operation is high due to its unequal pull-up and pull-down

delays, but IG mode design has low leakage power due to its architecture and SG mode circuit has high leakage power.

TABLE 4. SIMULATION RESULT OF FINFET VS CMOS BASED 6T SRAM

Parameters (VDD = 0.8 V)	**SG Mode - 6T SRAM**	**IG Mode - 6T SRAM**	**CMOS - 6T SRAM**
Dynamic Power (W)	1.40e -04	1.38e -04	3.37e -04
Leakage Power (W)	1.32e -06	1.01e -06	3.19e -06
Delay –Write operation (ps)	27.3	32.7	29.1
Delay -Read operation (ps)	21.5	27	23.4
SNM of write(mV)	160	172	125

VI. CONCLUSION

SRAM based memory designs are too sensitive for transistor density, so SRAM based design has been chosen as ideal design for comparing the performance of 22nm CMOS and FINFET. From the work carried out in this paper, the FINFET and CMOS based design device parameters are observed that the thickness of fin and channel 8nm and 8.6nm respectively, thickness of oxide 1.05nm and 1.4nm for NMOS based FINFET and CMOS design correspondingly.

The 6T SRAM has been modeled for SG mode as well as IG mode of FINFET and saturation and linear current for different front gate bias (V_{FG}) and back gate bias (V_{BG}) also calculated with its drain current (I_{DS}). To obtain the accurate result of SRAM, transistor sizing should be considered as a significant parameter which is identified M1 and M3 as 90nm, M2 and M4 as 120nm and access transistors M5 and M6 are identified as 180nm.

The final comparison of bulk CMOS based 6T SRAM and FINFET based 6T SRAM for SG/IG mode has been carried out and leakage power, dynamic power, delay for writing and reading operation, and SNM for write operations are calculated and tabulated in table 4. From this table, we can conclude the delay of CMOS based SRAM design is more for read and write operation compared to FINFET based SG/IG modes. Among FINFET based SG and IG modes, SG mode design is giving better performance at all the load level since IG mode has uneven pull-up and pull-down transistor which causes the unequal delay in the circuit.

REFERENCES

[1] Brain Swahn and Soha Hassoun (July 2006), *Gate Sizing: FinFETs vs 32nm Bulk MOSFETs*, In proceedings of DAC, Vol 2. pp. 218-224, California, USA.

[2] Y.Omura, S.Cristovoveanu, F. Gamiz, B-Y. Nguyen (2009), *Advanced FinFET Devices for sub-32nm Technology Nodes: Characteristics and Integration Challenges*, In proceedings of SoI Technology and Devices 14, Issue 4, pp.45–54.

[3] D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T.-J. King, J. Bokor, and C. Hu.(1998) *A folded-channel MOSFET for deep-sub-tenth micron era*, International Electron Devices Meeting.

[4] Nirmal, Vijayakumar and Sam Jabaraj (2010), *Nand Gate using FINFET for Nano-Scale Technology, In International Journal of Engineering Science and Technology*, Vol. 2(5), pp-1351-1358.

[5] Alexei Nazarow, J. P. Colinge et al (2011). *Semiconductor-On-InsulatorMaterial for Nanoelectronics Applications*, Springer Heidelberg Dordrecht, London.

[6] Lourts Deepak A. and Likhitha Dhulipalla (2011), *Design and Implementation of 32nm FINFET based 4x4 SRAM cell array using 1-bit 6T SRAM*, In Proceedings of the International conference on Nanoscience, Engineering and Technology, ISBN:978–1–4673–0072–8, pp. 218 – 221.